Composite Line Driver With Low Distortion

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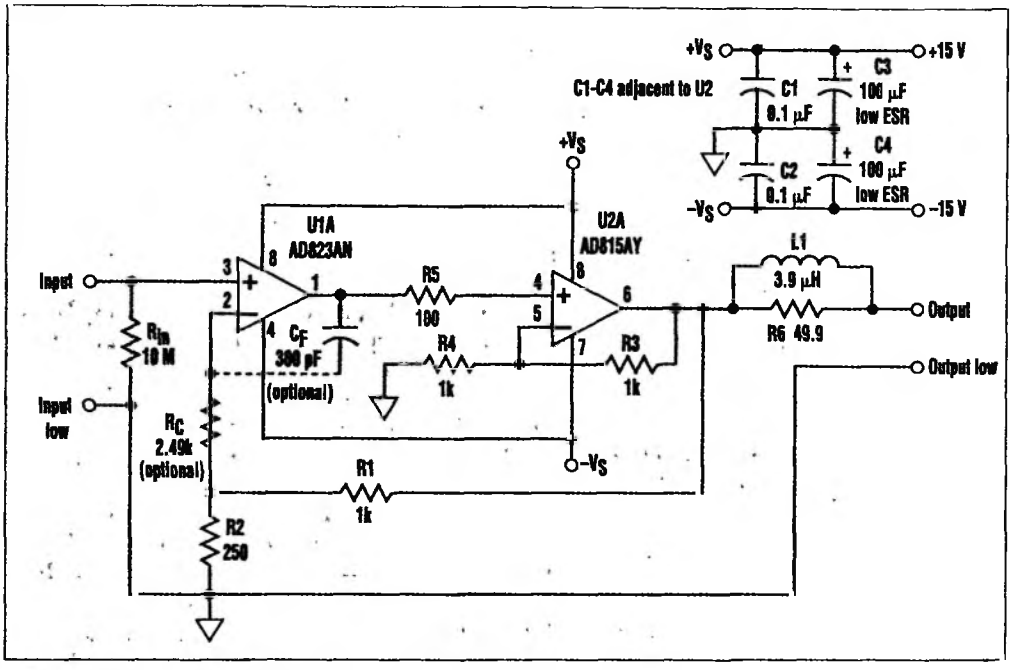
Outwardly, audio line drivers seem rather simple, yet their design can be problematic. They must be capable of appreciable output levels in terms of voltage swing and/or current levels. At the same time, they must be well behaved into more difficult loads, such as capacitive lines, or low impedances like headphones. Meeting these requirements isn't always trivial.

Unlike video systems, audio transmissions typically eschew terminated lines for transmission. Therefore, long signal lines usually appear capacitive to a driver, and the concepts of capacitive-load (cap-load) isolation are very important. Such loads demand high peak-current capability and good linearity, with no instability due to cap loading. And lower-impedance loads (below about 100 Ω) can demand unusually high output current from the amplifier, up to several hundred milliamperes. These levels can give rise to a number of associated problems such as gain loss, distortion rise, thermally related effects such as crosstalk between channels, and low-frequency distortion.

Often, single- or dual-IC op amps are used as simple driver stages for audio lines, usually with five- to ten-fold voltage gains. However, a simply configured stage has some requirements that conflict—it must drive low-impedance and/or reactive loads, yet it can't distort. It should operate stably from medium- to high-Z sources without changes in dc offset, noise, and distortion as the source impedance changes (with volume, for example). But, high output currents can trigger thermal feedback in both single and dual ICs. If present, this can be a problem for both dc and low-frequency ac signals, and generate crosstalk between channels.

Today's better FET-input op amps display good dc specs—low offset voltage and bias currents of just a few picoamperes—allowing a line driver stage to be completely dc-coupled. But few FET input IC op amps do well driving very-low-impedance loads. Some bipolar op amps exhibit much greater output drive. But, nonetheless, care must be taken about thermal effects and other distortions, making an optimum circuit choice challenging.

Fortunately, a technique of combining the best aspects of two different amplifiers into a single *composite* amplifier structure produces real dividends for audio and other high-current drivers. In this case, a FET input IC is combined with a high-current, wideband output stage.[1] Thus, the positive features of dissimilar, physically separate ICs can be exploited. Figure 1 shows a low-distortion composite amplifier, suitable for drivers with peak output currents up to 500 mA.



1 This low-distortion driver circuit delivers up to ±0.5 A and is suitable for loads of 10 Ω and up. Using a low-offset, low-bias-current input stage, the driver can be entirely direct-coupled.

In the circuit, stage U1 provides the bulk of the overall amplifier open-loop gain and determines the dc input characteristics. U1 is loaded only by the high-impedance input of U2, which helps linearity. U2 provides primarily the high current output, with some additional voltage gain via local feedback. Quite importantly, thermal effects occurring in U2 become relatively negligible in this hookup. Because the overall feedback loop includes U2, the gain of U1 reduces stage 2 nonlinearities as U2 undergoes heating/cooling cycles. Because U1 is thermally isolated from U2, and supplies a low load current, it's also isolated from load-related thermal effects.

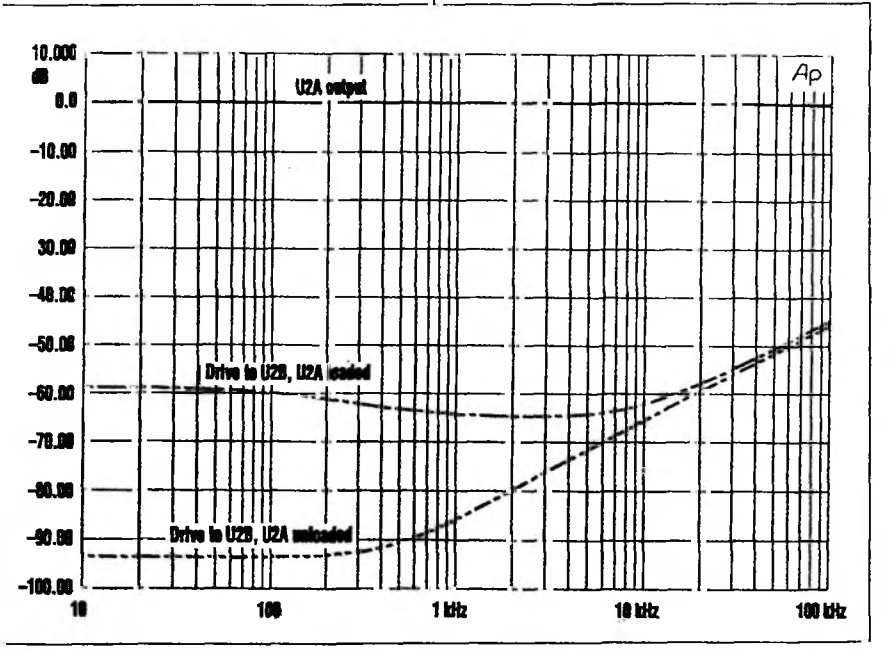
The overall amplifier operates at a voltage gain "G" of 5 (in this case), set by R1 and R2, as in a conventional noninverting amplifier:

$$G = 1 + (R1/R2)$$

Since U2 is a current-feedback amplifier, local feedback resistor R3 has a preferred value for stability purposes, 499 Ω (or more). Here, 1-kΩ R3/R4 values are used for simplicity, making the local gain of U2 = 2 (note that an R3 resistor is used even when U2's gain is unity).

The circuit's ability to minimize thermal effects includes both the U1-U2 forward signal path, and Left-Right channel coupling with dual devices. With U2 a dual IC, the effects of heavy currents from a driven channel can potentially be thermally coupled into the undriven channel—through the substrate. Figure 2, a 10-Hz-to-100-kHz swept level versus frequency display, is a plot taken with channels A and B operating, but only channel A driven. This illustrates the thermal-coupling effects from the active A output to the inactive B output. With channel A driving 2 V rms into a 25-W load, U2A dissipates sufficient power to induce an error signal into U2B. However, because of the overall servo loop and the fact that U1B isn't driven, the U2B output node will show little or no error, since driver U1B servos it to a null condition.

Nevertheless, the channel B thermal errors, caused by changes in the input characteristics of U2B, do appear *inside the loop*, and can easily be seen at the output of U1B. In the curves plotted in Figure 2, the upper curve is for 2 V rms = 0 dB, the channel A reference output. The two lower curves reflect the drive to U2B, with channel A's output both loaded and unloaded. For the loaded case, the drive to the B channel output stage changes about 30 dB over that of the unloaded case at fre-



2 The effects of thermal channel-to-channel coupling in the U2A and U2B power-output stages are depicted in this plot of relative response versus frequency. The uppermost curve is the channel A output from U2A driving a 25-Ω load at 2 V rms. Without the 25-Ω load, the drive to U2B reduces more than 30 dB (lower curves).

quencies below 1 kHz, indicating that thermal effects aren't solely confined to the very low frequencies.

Raw power dissipation capability also is important with power-handling circuits like the one described here. For example, on supplies of ±15 V, U2 will dissipate a fairly large power level of 900 mW without a signal. The power tab package of the device should be used with a dual-sided copper pc-board plane area of 2000 mm^2, which provides a thermal resistance of 16 °C/W. This heat sink will allow total U2 dissipations of nearly several watts in a 70-°C ambient temperature. Power-supply strategy also is important, and the supply decoupling shown should be considered a minimum. Obviously, power-supply requirements will be in inverse proportion to the load impedance.

When used alone (that is, without L1), output resistor R6 in this circuit should be 10 Ω or more to isolate the buffer from capacitive loading. For an extra safety margin against possible instability due to capacitive loads, this resistor should be made as high as feasible, such as the 50 Ω shown. But when driving very low impedances, such as 8 Ω and up, a simple resistive isolation scheme just won't work. In such cases, a fixed resistor of 30 to 50 Ω can be shunted with a small 3.9-μH inductor, such as a Miller 4608.[2] Alternately, the JT-OLI-2 isolator performs a similar function in one component.[3] If bandwidth reduction is needed, this can be accomplished with the optional capacitor C_F.

Very-low-resistance iron-core or ferrite-based chokes may seem attractive for the isolator application, in particular ferrite beads. However, these must be carefully evaluated for distortion due to nonlinear magnetics when handling high signal currents. For this reason, aircore chokes are preferred for L1. Both inductors mentioned have about 0.3 Ω of resistance, providing reasonably-low loss for most loads. At high frequencies, the net impedance of the RL network levels off to the value of the shunt resistor, providing good isolation to the amplifier. The circuit with L1 is stable into capacitive loads of at least 10 nF.

Due to the nonlinear C/V characteristic of JFET input op amps, their harmonic distortion performance can be a function of source impedance.[4,5] This mechanism can cause higher-than-desired distortion when such amplifiers operate with appreciable common-mode (CM) voltages, or as followers (the case here). A circuit solution that addresses this distortion provides an optional equalizing resistance, R_C, placed between the feedback divider and the input to U1. The value is chosen so that R_C, plus R1 paralleled with R2, is equal to the net source impedance at the signal input. This measure ensures that distortion developed due to applied CM voltage is predominantly CM and not differential, thus minimizing distortion.

The circuit tests well using loads as low as 10 Ω, and can deliver 4.5 V rms to such a load, with THD+N on the order of 0.0025% below 20 kHz (tested using the R_C value of Figure 1, with a source impedance of about 2.7 kΩ). This operating point would reflect a worst-case load impedance and current for U2, which has an internal current limit of 500 mA minimum, when used on ±15-V supplies. Of course, for higher impedances, much greater voltage swing is available. ED

References:
1. W. Jung, S. Wurcer, "A High Performance Audio Composite Line Driver Stage" within Chapter 5, *1992 Amplifier Applications Guide*, Analog Devices.
2. Type 4602-4612 series phenolic core chokes, J.W. Miller, 306 E. Alondra Blvd., Gardena, CA, (310) 515-1720
3. JT-OLI-2 Output Load Isolator, Jensen Transformers Inc., 7135 Hayvenhurst Ave., Van Nuys, CA 91406, (818) 374-5857.
4. W. Jung, "Op Amp Device/Topology Related Distortions," Chapter 8 of *System Applications Guide*, Analog Devices, 1993.
5. W. Jung, "S&K Distortion Culprit?," *Electronics World & Wireless World* (letters page), January 1996.